PRELIMINARY

2817

16K (2K X 8) ELECTRICALLY ERASABLE PROM

- **Self Timed Byte Write with Automatic Erase**
- **Direct Microprocessor Interface Capability**
- **Static 21 Volt V_{PP}**
- **Reduces Support Component Requirement by 70% to 90% Over 2816 and 2815**
- **Fast Byte Write Time:**
  —Write Typical, 5 mS
  —Cycle Typical, 10 mS
- **Very Fast Read Access Time:**
  —2817, 250 nS
  —2817-3, 350 nS
  —2817-4, 450 nS
- **Reliable Intel FLOTOX E^2PROM Technology**

The Intel 2817 is a 16,384 bit Electrically Erasable Programmable Read Only Memory. Like the Intel 2816 and 2815, it has completely Non-Volatile Data Storage. However, in addition, it offers a high degree of integrated functionality which enables in-circuit byte writes to be performed with minimal hardware and software overhead. The Intel 2817 is a product of Intel's advanced E^2PROM technology and uses the powerful HMOS*-E process for reliable, *non-volatile,* data storage.

The Intel 2817 eliminates all the interfacing hardware logic and firmware required to perform data writes. The device has complete self-timing which leaves the processor free to perform other tasks until the 2817 signals 'Ready.' With a transparent erase before write, the user benefits by saving an erase command contributing to efficient usage of system processing time. On chip latching further enhances system performance.

The Intel 2817's very fast read access time makes it compatible with high performance microprocessor applications. It uses Intel's proven 2-line control architecture which eliminates bus contention in a system environment. Combining these features with the 2817's 'Ready' signal makes the device an extremely powerful, yet simple to use, E^2 memory—available to the designer today.

The density, and level of integrated control, makes the Intel 2817 suitable for users requiring low hardware overhead, high system performance, minimal board space and design ease. Designing with, and using the 2817, is extremely cost effective as 70% of the required voltage and interfacing hardware required for other E^2PROM devices has been eliminated. See Figures 1, 2, and 3 for the Intel 2817's block diagram, pinout, and simple interface requirements.

*HMOS-E is a patented process of Intel Corporation.

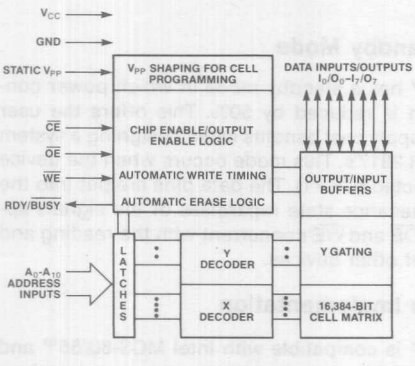

Figure 1. 2817 Functional Block Diagram

PIN NAMES

A_0-A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	DATA OUTPUTS
I_0-I_7	DATA INPUTS
V_{PP}	STATIC PROGRAMMING VOLTAGE
RDY/$\overline{BUSY}$	DEVICE READY/BUSY
TC	TIMING CAPACITOR
N.C.	NO CONNECT

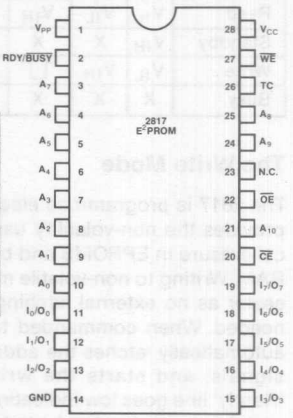

Figure 2. 2817 Pin Configuration

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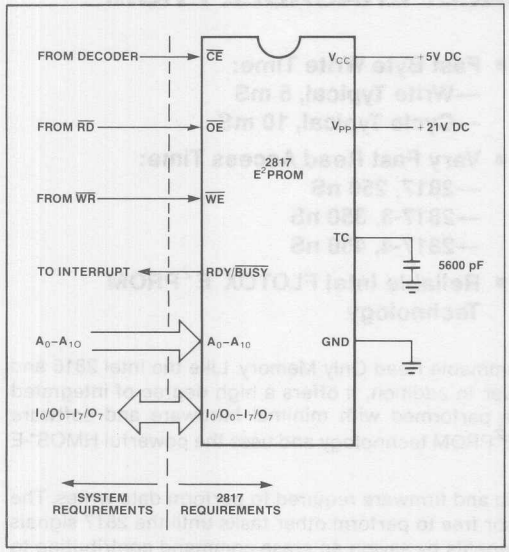


Figure 3. Simple 2817 Interface Requirements

DEVICE OPERATION

The Intel 2817 has 4 modes of user operation which are detailed in Table 1. All modes are designed to enhance the 2817's functionality to the user and provide total Intel E^2PROM microprocessor compatibility.

Table 1. V_{CC} = +5V, V_{PP} = +21V

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I_0/O_0-I_7/O_7	RDY/$\overline{BUSY}$
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	V_{OH}
Standby	V_{IH}	X	X	High Z	V_{OH}
Write	V_{IL}	V_{IH}	⊓	D_{IN}	V_{OH}
Busy	X	X	X	High Z	V_{OL}

The Write Mode

The 2817 is programmed electrically in-circuit, yet it provides the non-volatility usually obtained by optical erasure in EPROMS and by batteries with CMOS RAM. Writing to non-volatile memory has never been easier as no external latching, erasing or timing is needed. When commanded to byte write, the 2817 automatically latches the address, data, and control signals, and starts the write. Concurrently, the 'Ready' line goes low indicating that the 2817 is Busy and that it can be deselected to allow the processor to perform other tasks. During the write, the static V_{PP} is used to perform an automatic byte erase, then write. The 2817 has on-chip data verification to ensure successful byte programming. This is achieved by comparing the data written to the cell with the data latched on chip during the write request. The timing capacitor (TC) is used by the 2817 to generate the correct internal V_{PP} rise time constant for cell programming. Its value is 5600 pF ±10%.

Should a regulated +24V DC be available in the system, the circuit shown in Figure 4 can be used to provide the required V_{PP} voltage. Should +24V not be available, the implementation in Figure 5 can be used to provide the static programming voltage.

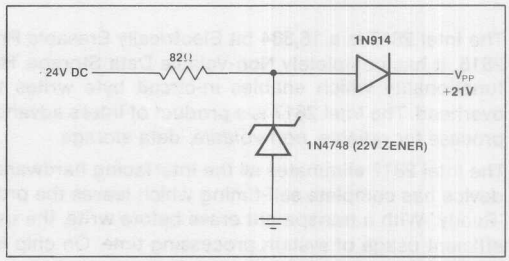


Figure 4. Voltage Stepdown from +24V DC to +21V DC

The Read Mode

One aspect of the 2817's high performance is its very fast read access time—typically less than 250 ns. It's read cycle is similar to that of EPROMS and static RAM's. It offers a 2 line control architecture to eliminate bus contention. The Intel 2817 can be selected using decoded system address lines to $\overline{CE}$ and then the device can be read, within the device selection time, using the processor's $\overline{RD}$ signal connected to $\overline{OE}$.

The Standby Mode

The 2817 has a standby mode in which power consumption is reduced by 50%. This offers the user power supply cost benefits when designing a system with Intel 2817's. This mode occurs when the device is deselected ($\overline{CE}$=1). The data pins are put into the high impedance state regardless of the signals applied to $\overline{OE}$ and $\overline{WE}$ concurrent with the reading and writing of other devices.

System Implementation

The 2817 is compatible with Intel MCS-80/85™ and iAPX-86/88 Microprocessors. It requires no interface circuitry and minimal support circuitry. Figure 6 shows an example of the 2817 interfaced to an Intel 8085. The Intel 8282 de-multiplexes the address lines

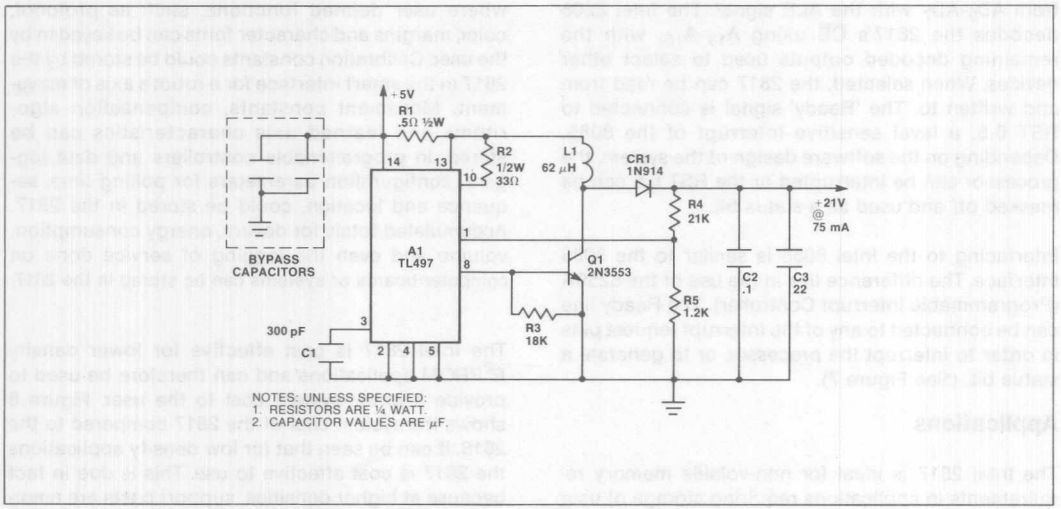


Figure 5. Step-up Regulator Converts +5V to +21V

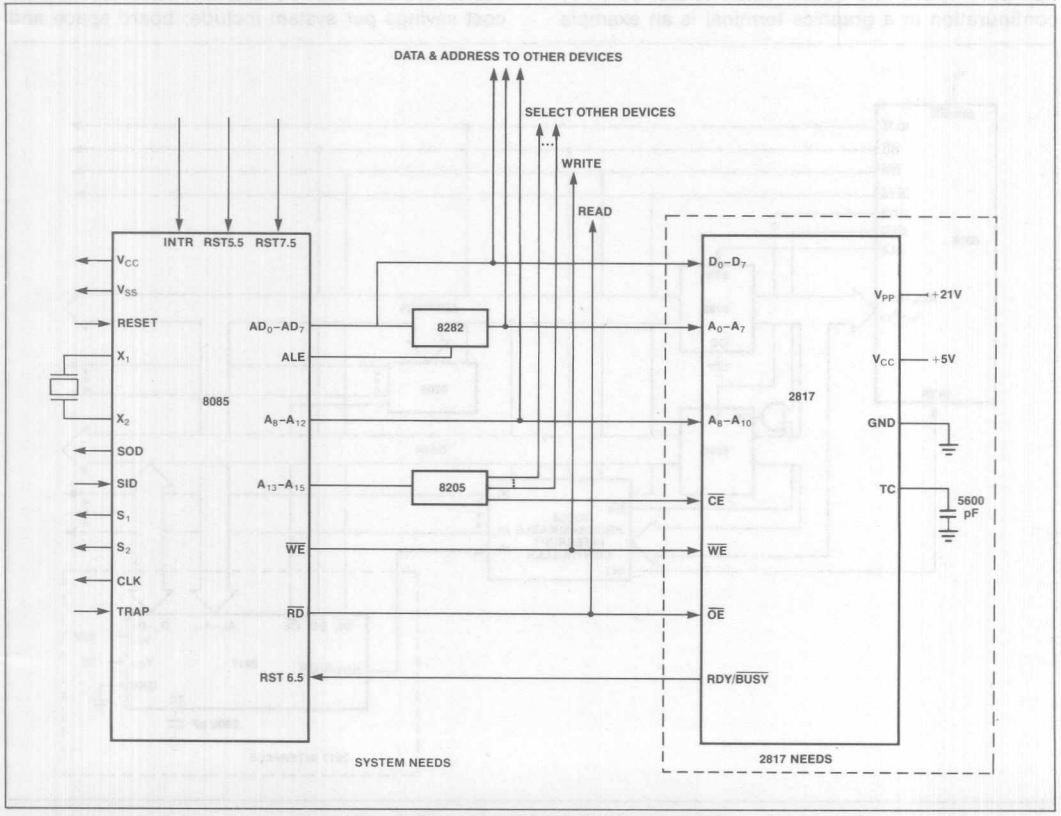


Figure 6. 2817/8085 Interface Example

from AD_0-AD_7 with the ALE signal. The Intel 8205 decodes the 2817's $\overline{CE}$ using A_{13}-A_{15}, with the remaining decoded outputs used to select other devices. When selected, the 2817 can be read from and written to. The 'Ready' signal is connected to RST 6.5, a level sensitive interrupt of the 8085. Depending on the software design of the system, the processor can be interrupted or the RST 6.5 can be masked off and used as a status bit.

Interfacing to the Intel 8088 is similar to the 8085 interface. The difference lies in the use of the 8259A (Programmable Interrupt Controller). The Ready line can be connected to any of the interrupt request pins in order to interrupt the processor, or to generate a status bit. (See Figure 7).

Applications

The Intel 2817 is ideal for non-volatile memory requirements in applications requiring storage of user defined functions, calibration constants, configuration parameters and accumulated totals. Soft key configuration in a graphics terminal is an example where user defined functions, such as protocol, color, margins and character fonts can be keyed in by the user. Calibration constants could be stored by the 2817 in the smart interface for a robot's axis of movement. Movement constants, compensation algorithms and learned axis characteristics can be stored. In programmable controllers and data loggers, configuration parameters for polling time, sequence and location, could be stored in the 2817. Accumulated totals for dollars, energy consumption, volume and even the logging of service done on computer boards or systems can be stored in the 2817.

The Intel 2817 is cost effective for lower density E^2PROM applications and can therefore be used to provide a lower system cost to the user. Figure 8 shows the system cost of the 2817 compared to the 2816. It can be seen that for low density applications the 2817 is cost effective to use. This is due in fact because at higher densities, support costs are amortized, or spread over, many devices—thus reducing overall system cost. The user will find that tangible cost savings per system include: board space and

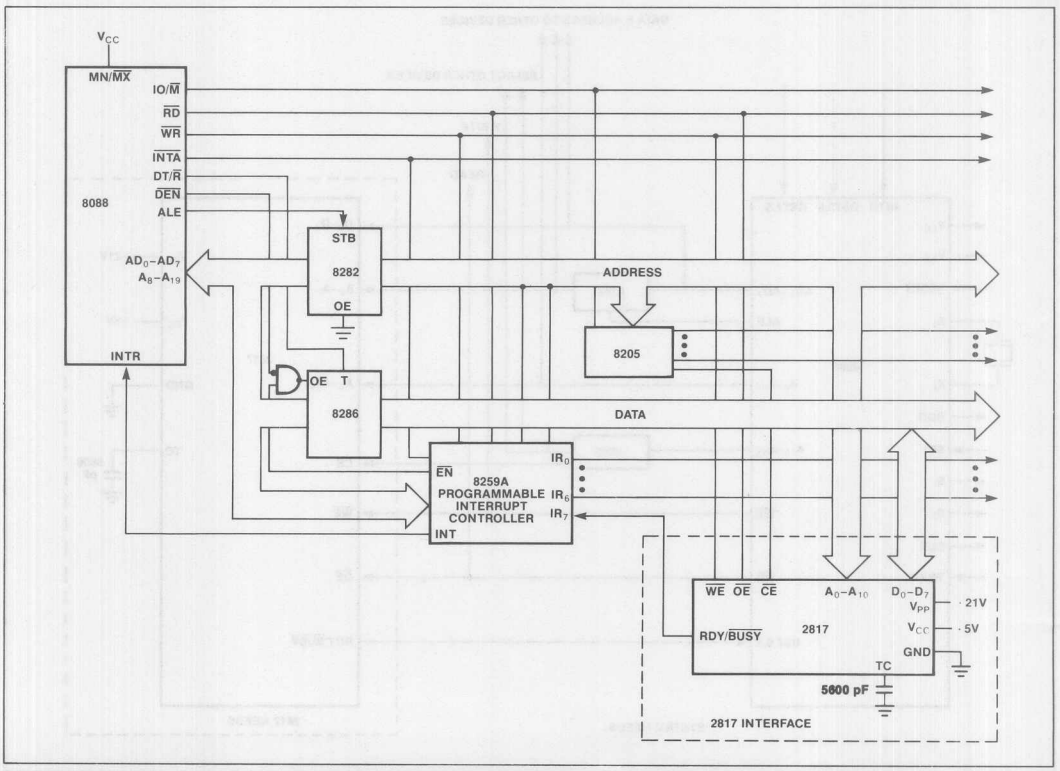


Figure 7. 2817/8088 Interface Example

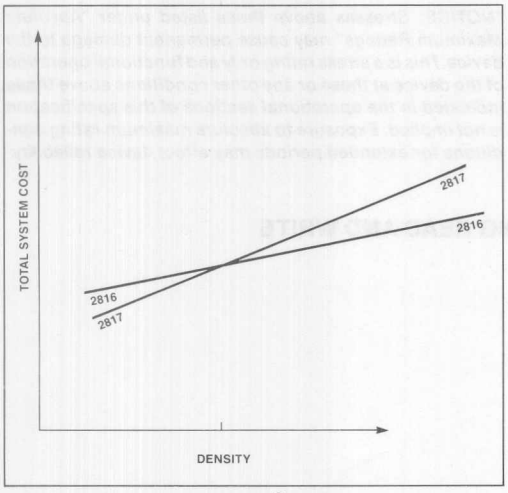


Figure 8. Total E^2 System Cost

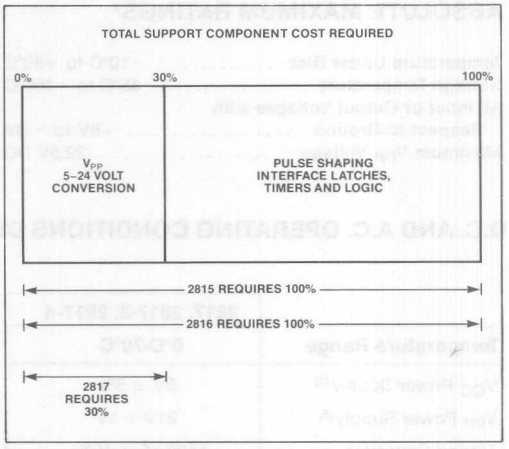


Figure 9. Support Components Cost Requirements for E^2PROMs

component reductions, reduced assembly costs, savings in inventory costs, handling costs and Quality Assurance. The designer will find the 2817 reduces design time by a sizeable factor over the 2816 due to the integration of timing, logic, latching and V_{PP} shaping circuitry.

The 2817 will also open up new applications in environments where flexible parameter/data storage could not be implemented before. For example, applications with board space constraints are ideal for the 2817 as it requires only 25% of the board space compared to the 2816 and 2815. This is due to the reduction of all components required except the V_{PP} generator. Figure 9 shows the reduction of support component costs of the 2817 over the 2816, 2815. Figure 10 illustrates the system board space requirements of the 2817, 2816, and 2815.

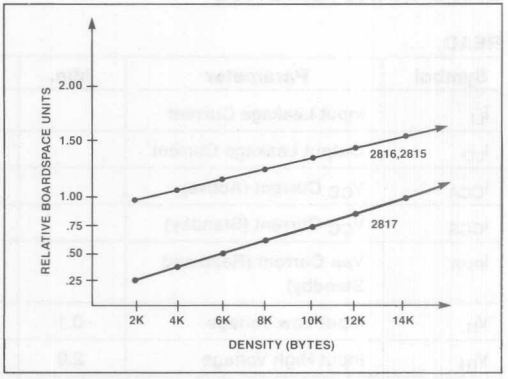


Figure 10. System Board Space Requirement

Write Time Characteristics

The 2817's internal write cycle contains an automatic erase feature. The 2815 and 2816 do not have this capability—they must be given an external erase cycle prior to a write. The 2815 has a write time specification of 50 ms minimum—that is, the device can not be written or erased any faster than 50 ms. The 2816 has a specification of 10 ms. Typically, these devices will write in times less than 50 or 10 ms, but the worst case bit defines the minimum specification.

The 2817, however, automatically determines when a byte has been successfully written and therefore, average write times are significantly faster. The 2817's internal cycle consists of an automatic 5 ms (typical) erase followed by a 5 ms (typical) write. The total cycle is then typically 10 ms. This cycle is the time that Ready is held low by the device. The 2817 maximum specification is 75 ms, 37.5 ms for erase and 37.5 ms for write.

The 2817 compares directly to the 2815—except 25 ms of processing time is gained (the 2815 requires a 50 ms erase then 50 ms write for a 100 ms cycle). A future device will be offered from Intel (the 2817-xx) that will write in a maximum of 20 ms, just as the present 2816.

To summarize, because of rapid on-average write/erase times, and sophisticated internal control, the 2817 will write on average in 10 ms. This compares with 20 ms for the 2816 and 100 ms for the 2815.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +100°C
All Input or Output Voltages with
Respect to Ground ..... +6V to −.3V
Maximum V_{PP} Voltage ..... 22.5V DC

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND A.C. OPERATING CONDITIONS DURING READ AND WRITE

	2817, 2817-3, 2817-4
Temperature Range	**0°C-70°C**
V_{CC} Power Supply (1)	5V ± 5%
V_{PP} Power Supply (5)	21V ± 1V
Timing Capacitor	5600 pF ± 10%

D.C. CHARACTERISTICS

READ

Symbol	Parameter	Min.	Typ(2)	Max.	Units	Test Conditions
I_{LI}	Input Leakage Current			10	μA	V_{In} = 5.5V
I_{LO}	Output Leakage Current			10	μA	V_{Out} = 5.5V
I_{CCA}	V_{CC} Current (Active)		100	150	mA	$\overline{OE} = \overline{CE} = V_{IL}$
I_{CCS}	V_{CC} Current (Standby)			60	mA	$\overline{CE} = V_{IH}$
I_{PPR}	V_{PP} Current (Read and Standby)			8	mA	V_{PP} = 22V
V_{IL}	Input Low Voltage	−0.1		.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 μA

WRITE

Symbol	Parameter	Min.	Typ.(2)	Max.	Units	Test Conditions
V_{PP}	Write Voltage	20		22	V	
I_{PPW}	V_{PP} Current (Write)			15	mA	RDY/$\overline{BUSY}$ = V_{OL}
I_{CCW}	V_{CC} Current (Write)			150	mA	RDY/$\overline{BUSY}$ = V_{OL}

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Symbol	Parameter	Typ.(2)	Max.	Units	Test Conditions
C_{IN}	Input Capacitance	5	10	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance		10	pF	V_{OUT} = 0V
CV_{CC}	V_{CC} Capacitance		500	pF	$\overline{OE}$ = $\overline{CE}$ = V_{IH}
CV_{PP}	V_{PP} Capacitance		50	pF	$\overline{OE}$ = $\overline{CE}$ = V_{IH}

A.C. TEST CONDITIONS

Output Load ..... 1 TTL gate + C_L = 100 pF
Input Pulse Levels ..... 0.45 to 2.4V
Timing Measurement
Reference Level ..... Input 1V and 2V,
Output .8V and 2V

A.C. CHARACTERISTICS

READ

Symbol	Parameter	2817 Limits			2817-3 Limits			2817-4 Limits			Units	Test Conditions
		Min.	Typ.(2)	Max.	Min.	Typ.(2)	Max.	Min.	Typ.(2)	Max.		
t_{ACC}	Address to Output delay		200	250		300	350		400	450	nS	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
t_{CE}	$\overline{CE}$ to Output Delay		200	250		300	350		400	450	nS	
t_{OE}	Output Enable to Output Delay	10		100	10		120	10		150	nS	
t_{DF}	Output Enable High to Output Float	0		80	0		100	0		130	nS	$\overline{CE}$ = V_{IL}
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	20			20			20			nS	$\overline{CE}$, $\overline{OE}$ = VIL

WRITE

Symbol	Parameter	Min.	Typ.(2)	Max.	Units	Test Conditions
t_{AS}	Address to write set-up time	20			nS	
t_{CS}	$\overline{CE}$ to write set-up time	20			nS	
t_{WP}	Write pulse width	100			nS	
t_{AH}	Address hold time	50			nS	
t_{DS}	Data set-up time	50			nS	
t_{DH}	Data hold time	20			nS	
t_{CH}	$\overline{CE}$ hold time	50			nS	
t_{DB}	Time to Device Busy			75	nS	
	External Processor Timing					
	CPU Supervision Time			200	nS	
	Internal 2817 Timing					
	Internal Erase Time		5	37.5	mS	

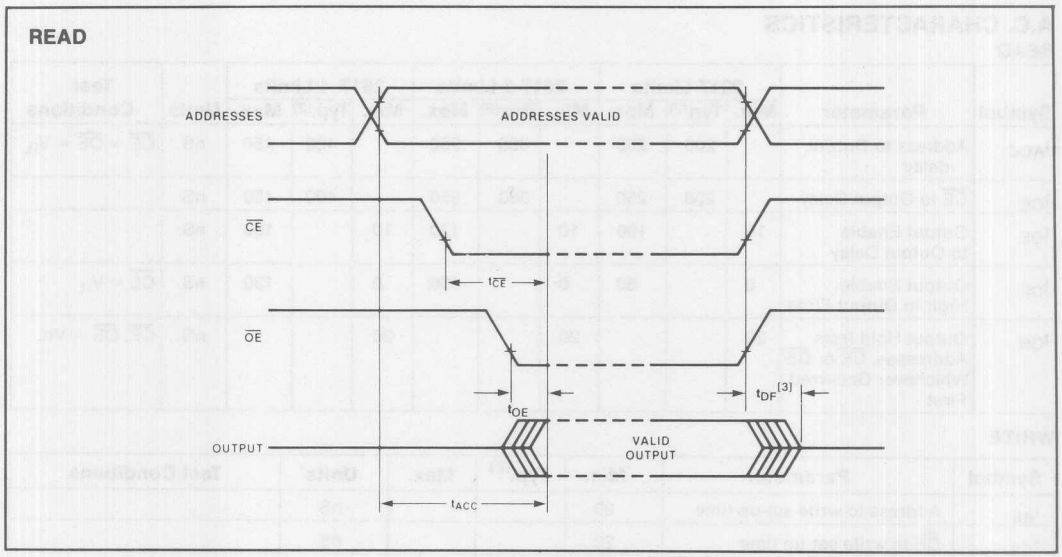
WRITE (Continued)

Symbol	Parameter	Min.	Typ.(2)	Max.	Units	Test Conditions
	Internal Write Time		5	37.5	mS	
	External READY Timings					
t_{WR}	Byte Write Cycle Time (2817)		10	75	mS	
t_{WR}	Byte Write Cycle Time (2817-xx)		10	20	mS	

NOTES:
1. The $\overline{WE}$ input must track V_{CC} as it rises from the 5V level to prevent spurious write sequences.
2. This parameter only sampled and not 100% tested.
3. t_{DF} is specified from OE or CE, whichever occurs first.
4. A faster write speed to parallel the 2816 will be offered.
5. V_{PP} should only be applied when V_{CC} is valid.

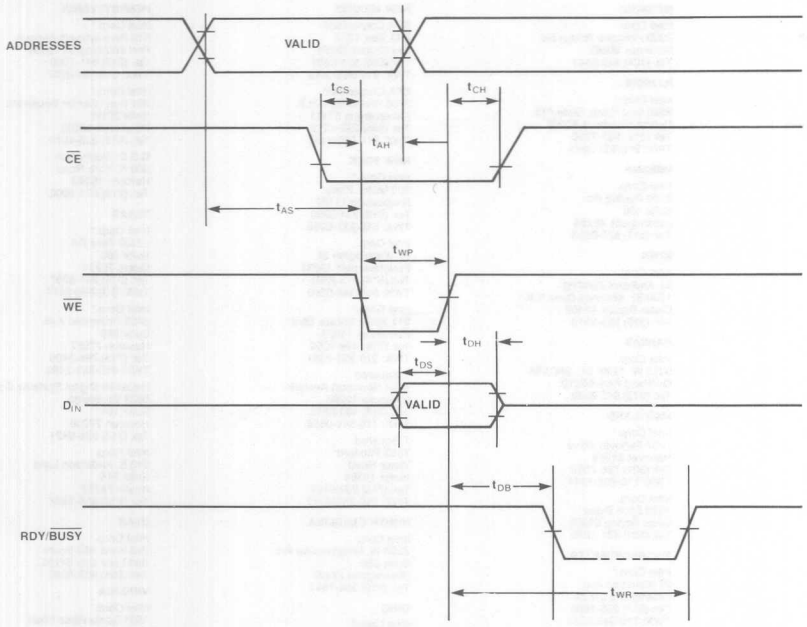
WAVEFORMS

READ



WAVEFORMS (Continued)

WRITE



AVAILABLE LITERATURE

The Intel E^2PROM family of devices, the 2815, 2816 and 2817 is supported by many Application Notes and Application Briefs. Topics covered range from Intel E^2PROM Technology and Reliability to Design considerations and Applications support for Designers implementing large arrays of E^2PROMs.

A brief synopsis of some notes is given below as a reference to system designers and architects. These notes and more are available in the E^2PROM Family Applications Handbook II.

AP100—Reliability Aspects of a Floating Gate E^2PROM

AP101—The 2816 Electrical Description

AP102—2816 Microprocessor Interface Considerations

AP103—Programming E^2PROM with a Single 5-Volt Power Supply

AP107—Hardware and Software Download Techniques with 2816

AP135—8298 Integrated E^2 Controller

AP136—A Multibus-Compatible 2816 E^2PROM Memory Board

AP137—8298 Functional Specification and Firmware Description

AP138—A 2716 to 2816 Programming Socket Adapter

To obtain this book contact your local Field Sales office. (Order Number 210273) Your Field Applications Engineer is available to discuss all aspects of the Intel E^2 product line with you.